Lecture No 12

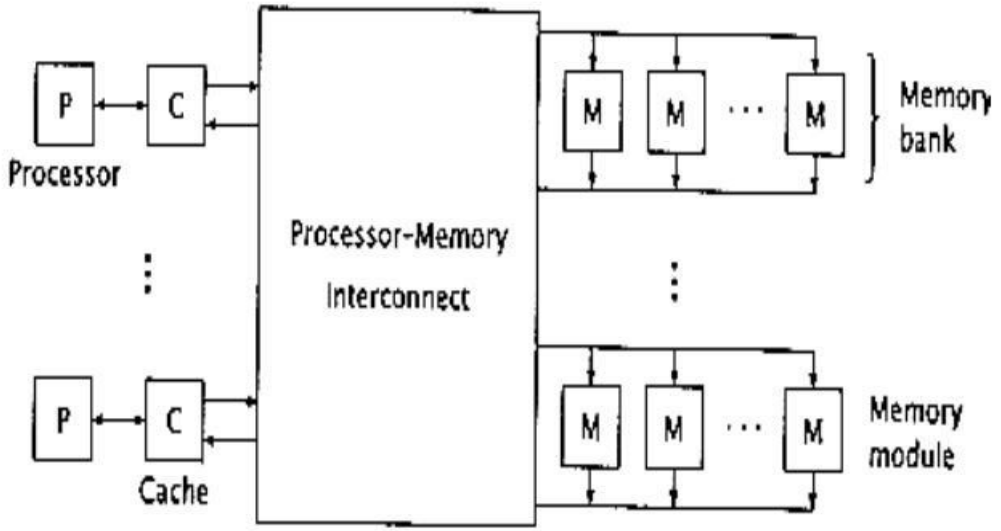
Memory System Design

Memory System

- There are two basic parameters that determine Memory systems Performance

1. **Access Time**: Time for a processor request to be transmitted to the memory system, access a datum and return it back to the processor.(Depends on physical parameter like ***bus delay***, ***chip delay*** etc.)
2. **Memory Bandwidth:** Ability of the memory to respond to requests per unit of time. (depends on memory system organization, No of memory modules etc.

Memory System Organization



Memory System Organization

- No. of memory banks each consisting of no of memory modules, each capable of performing one memory access at a time.
- Multiple memory modules in a memory bank share the same input and out put buses.
- In one bus cycle, only one module with in a memory bank can begin or complete a memory operation.
- Memory cycle time should be greater than the bus cycle time.

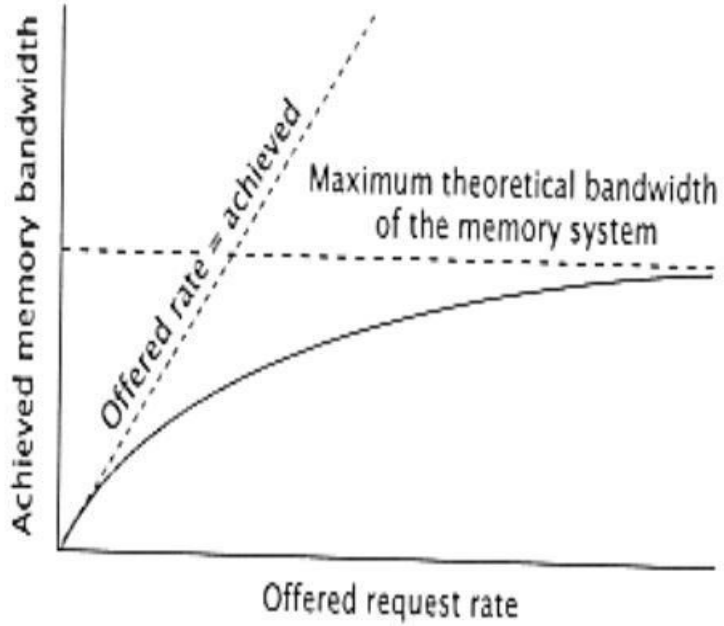
Memory System Organization

- In systems with multiple processors or with complex single processors, multiple requests may occur at the same time causing bus or network congestion.
- Even in single processor system requests arising from different buffered sources may request access to same memory module resulting in memory systems contention degrading the bandwidth.

Memory System Organization

- The maximum theoretical bandwidth of the memory system is given by the number of memory modules divided by memory cycle time.
- The ***Offered Request Rate*** is the rate at which processor would be submitting memory requests if memory had unlimited bandwidth.
- ***Offered request rate*** and ***maximum memory bandwidth*** determine maximum Achieved Memory Bandwidth

Achieved vs. Offered Bandwidth



Offered Request Rate:

- Rate that processor(s) would make requests if memory had unlimited bandwidth and no contention

Memory System Organization

- The *offered request rate* is not dependent on organization of memory system.
- It depends on processor architecture and instruction set etc.
- The analysis and modeling of memory system depends on no of processors that request service from common shared memory system.
- For this we use a model where ***n*** simple processors access ***m*** independent modules.

Memory System Organization

- Contention develops when multiple processors access the same module.
- A single pipelined processor making ***n*** requests to memory system during a memory cycle resembles the **n** processor ***m*** modules memory system.

The Physical Memory Module

- Memory module has two important parameters
  - ***Module Access Time***: Amount of time to retrieve a word into output memory buffer of the module, given a valid address in its address register.
  - ***Module Cycle Time***: Minimum time between requests directed at the same module.

Memory access Time is the total time for the processor to access a word in memory. In a large interleaved memory system it includes module access time plus transit time on bus, bus accessing overhead, error detection and correction delay etc.

Semiconductor Memories

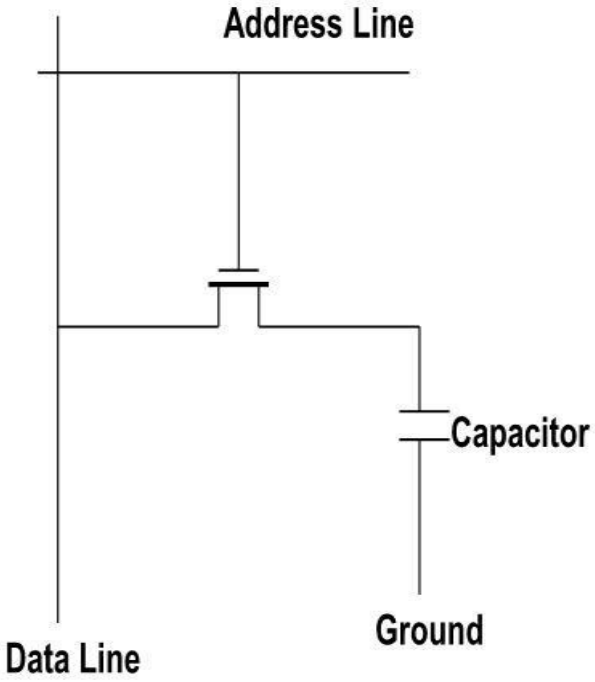
- Semiconductor memories fall into two categories.
  - Static RAM or SRAM
  - Dynamic RAM or DRAM

  The data retention methods of SRAM are static where as for DRAM its Dynamic.

  Data in SRAM remains in stable state as long as power is on.

  Data in DRAM requires to be refreshed at regular time intervals.

DRAM Cell



SRAM Vs DRAM

- SRAM cell uses 6 transistor and resembles flip flops in construction.
- Data information remains in stable state as long as power is on.
- SRAM is much less dense than DRAM but has much faster access and cycle time.
- In a DRAM cell data is stored as charge on a capacitor which decays with time requiring periodic refresh. This increases access and cycle times

SRAM Vs DRAM

- DRAM cells constructed using a capacitor controlled by single transistor offer very high storage density.
- DRAM uses destructive read out process so data readout must be amplified and subsequently written back to the cell
- This operation can be combined with periodic refreshing required by DRAMS.
- The main advantage of DRAM cell is its small size, offering very high storage density and low power consumption.